REMARKS

This is in response to the Office Action mailed on June 4, 2004, and the references cited therewith.

No claims are amended or cancelled. Claims 1-3 and 64-74 remain pending in this application.

§103 Rejection of the Claims

Claims 1-3 and 64-73 were rejected under 35 USC § 103(a) as being unpatentable over Yamada et al. (U.S. 5,617,537).

The rejection stated that Yamada shows, "a plurality of memory devices (21, e.g. 21-1, 21-2 and 21-3) associated with one processor." The rejection further stated that, "each of the memory devices 21-1, 21-2 and 21-3 is associated with any one of the processors 19-1, 19-2, and 19-3 and any one processor may access all of these memory deices via processor interconnect 25." The present rejection further states that, "upon review of the disclosure of the Yamada et al. system, it would have been obvious to one of ordinary skill in the art at the time of the invention to associate each memory device 21-1, 21-2, 21-3 with only one processor."

Yamada appear to show a plurality of memory devices 21-1, 21-2 and 21-3. Yamada also appears to show a plurality of processors 19-1, 19-2, 19-3. Applicant respectfully traverses the assertion of obviousness, using a single reference. Should the Examiner maintain this rejection, Applicant respectfully requests a reference, pursuant to M.P.E.P. Section 2144.03, which describes a plurality of memory devices associated with only one processor in order to support the Examiner's position.

Further, Applicant respectfully submits that modifying Yamada as suggested in the present Office Action to associate each memory device 21-1, 21-2, 21-3 with only one processor would destroy the stated purpose of Yamada. The Field of the Invention section in column 1, lines 10-16 refers to a "parallel multiprocessor system." If the suggested modification were made, the system of Yamada would cease to be both parallel, and multiprocessor. If a proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984); MPEP § 2143.01.

In contrast, claim 1 as amended includes a plurality of memory devices associated with only one processor, wherein each memory device includes a local address storage circuitry which stores a local address for identifying the storage circuitry's single associated memory device once an address assign command is decoded by a command decoder. Further in contrast, claims 64, 68, and 71 as amended include a processor, and a plurality of memory devices associated with only the processor.

Because Yamada does not show or make obvious every element of Applicant's independent claims, a 35 USC § 103(a) rejection is not supported by the references. Reconsideration and withdrawal of the rejection are respectfully requested with respect to claims 1, 64, 68, and 71. Additionally, reconsideration and withdrawal of the rejection are respectfully requested with respect to the remaining claims that depend therefrom as depending on allowable base claims.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6944 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 3rd day of September, 2004.

Amy Moriarty
Name

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Signature